Figure 1

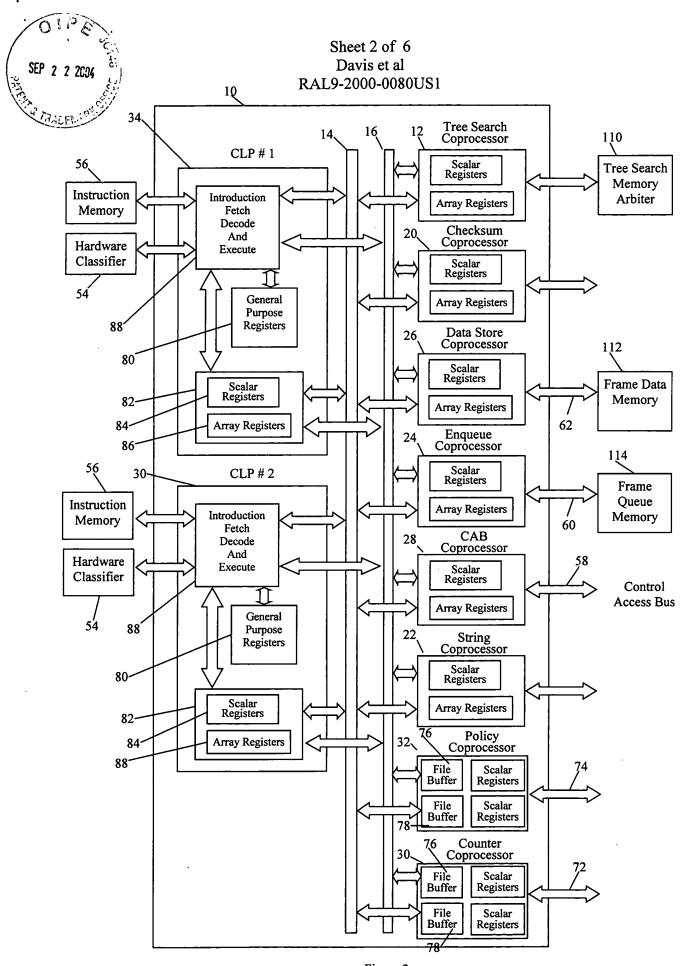


Figure 2



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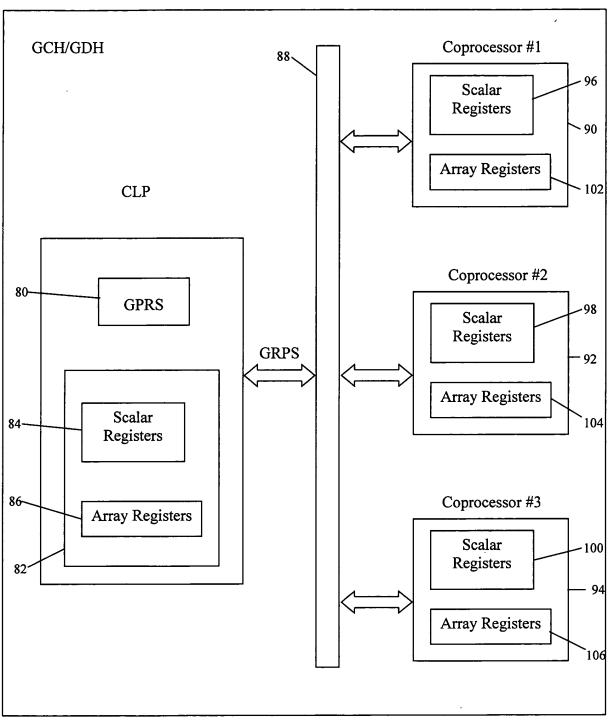


Figure 3



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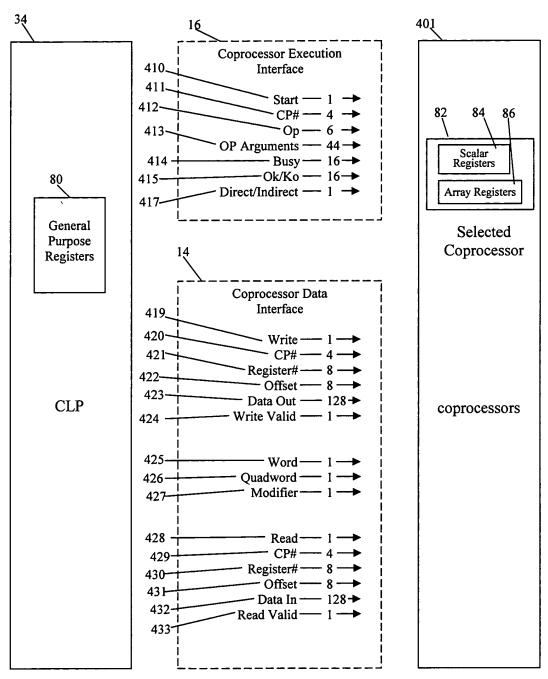
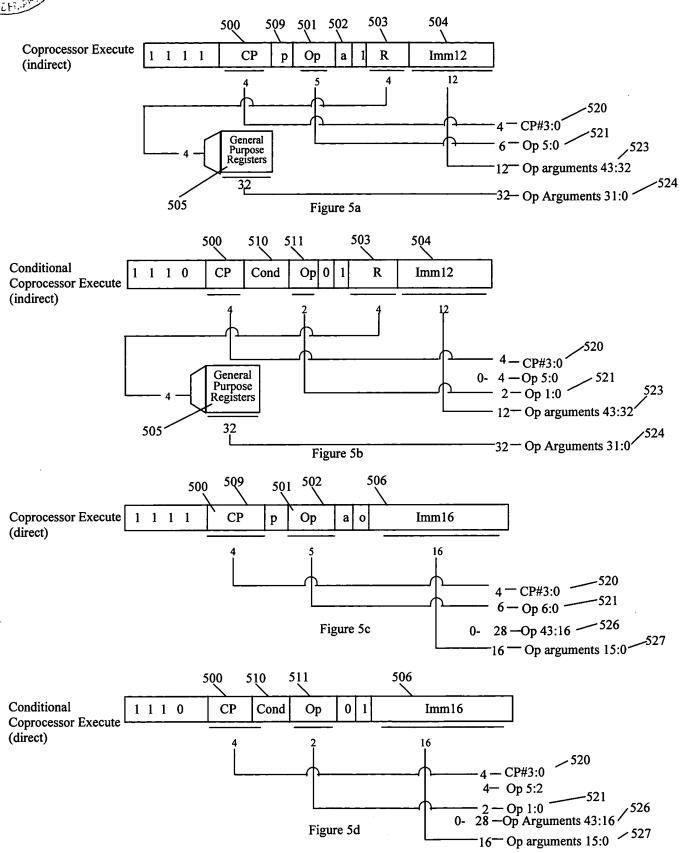


Figure 4



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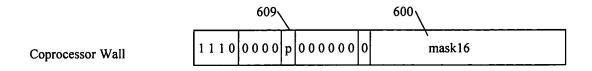


Figure 6a

Coprocessor Wall and Branch

1 1 1 0 | CP | p | 0 0 0 0 0 0 | 1 | target 16

Figure 6b